AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A serializer/deserializer (SERDES) circuit having built-in self-test (BIST) capabilities that is configured to perform jitter sensitivity characterization, comprising:

~~a CDR~~ a clock and data recovery (CDR) circuit coupled to said SERDES circuit that generates recovered clock and data from an incoming serial data stream;

a deserializer circuit connected to said CDR circuit to generate corresponding data (Parallel Data Out) and clock (DES clock) in a parallel format;

a programmable pattern generator generating BIST patterns;

a serializer circuit that receives either the BIST patterns or [[the]] input data (Parallel Data In) in a parallel format on [[its]] a data input of the serializer circuit and an external clock (SER clock) on [[its]] a clock input of the serializer circuit to generate a serial data stream;

a delay perturbation circuit for adding a perturbation delay to said serial data stream to produce a perturbed serial data stream;

a multiplexor circuit to output either the serial data stream or the perturbed serial data stream in a loop back to the CDR circuit;

a control logic circuit block coupled to said deserializer circuit to detect a start-of-frame pattern using a dedicated signal (FD) and coupled to the programmable pattern generator and the perturbation circuit.

2. (Original) The serializer/deserializer (SERDES) circuit according to claim 1 further comprising a calibration circuit coupled to the output of said delay perturbation circuit.

3. (Original) The serializer/deserializer (SERDES) circuit according to claim 1, wherein said delay perturbation circuit comprises a variable delay line and said perturbation comprises a variable delay.

4. (Original) The serializer/deserializer (SERDES) circuit according to claim 3, wherein said variable delay comprises a sudden increase or decrease of the delay value of said variable delay line.

5. (Currently Amended) The serializer/deserializer (SERDES) circuit according to claim 4, wherein said variable delay line comprises a plurality of [[DLL]] delayed locked loop (DLL) circuits, connected in series and coupled to said serial data stream.

6. (Currently Amended) The serializer/deserializer (SERDES) circuit according to claim 5, wherein the signal obtained at the output of said series of a plurality of [[DLL]] delayed locked loop (DLL) circuits is used as a calibration signal to be applied to a calibration circuit.

7. (Currently Amended) The serializer/deserializer (SERDES) circuit according to claim 6 further comprising a calibration circuit comprising a latch having its clock input connected to said calibration signal and a data input driven by the ~~serializer~~ external clock.

8. (Original) The serializer/deserializer (SERDES) circuit according to claim 7 wherein said calibration signal corresponds to a delay equal to the serializer clock half-period.

Claims 9-11. (Canceled)